A Review of Reliability Research on Nanotechnology

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***Abstract*—Nano-reliability measures the ability of a nano-scaled product to perform its intended functionality. At the nano scale, the physical, chemical, and biological properties of materials differ in fundamental, valuable ways from the properties of individual atoms, molecules, or bulk matter. Conventional reliability theories need to be restudied to be applied to nano-engineering. Research on nano-reliability is extremely important due to the fact that nano-structure components account for a high proportion of costs, and serve critical roles in newly designed products. This review introduces the concepts of reliability to nano-technology; and presents the current work on identifying various physical failure mechanisms of nano-structured materials, and devices during fabrication process, and operation. Modeling techniques of degradation, reliability functions, and failure rates of nano-systems are also reviewed in this work.**

***Index Terms*—Degradation, failure analysis, nano-reliability.**

ACRONYM[1]

AFM	Atomic Force Microscope
CMOS	Complementary Metal-Oxide-Semiconductor
CNF	Carbon Nano Fiber
CO	Carbon Monoxide
CONAN	Configurable Nanostructures for Reliable Nano Electronics
CVD	Chemical Vapor Deposition
ECC	Error Correcting Codes
ESD	Electrostatic Discharge
FA	Failure Analysis
FT-IR	Fourier Transform Infrared
GC/MS	Gas Chromatography-Mass Spectroscopy
GPC	Gel Permeation Chromatography
HCI	Hot Carrier Injection
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
MEMS	Micro-Electro-Mechanical Systems
MIM	Metal-Insulator-Metal
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MRAM	Magnetoresistive Random Access Memory
NAND	Negated Conjunction
nanoDAC	Nano Deformation Analysis by Correlation
NBTI	Negative Bias Temperature Instability
NDE	Nondestructive Evaluation
NEMS	Nano-Electro-Mechanical Systems
NF	Nano-Fibrous
nMOS	Negative-Channel Metal-Oxide-Semiconductor
NSET	The Nanoscale Science, Engineering, and Technology
PAS	Positron Annihilation Spectroscopy
PLLA	Poly-L-Lactide Acid
PMA	Post Metal Annealing
PRISM	Probabilistic Symbolic Model Checker
PS	Polystyrene
RF	Radio-Frequency
SC-Si	Single Crystal Silicon
SEM	Scanning Electron Microscopy
SIA	Semiconductor Industry Association
SOC	System-on-a-Chip
SPC	Statistical Process Control
SPM	Scanning Probe Microscopy
SRAM	Static Random Access Memory
SW	Solid-Walled
TDDB	Time-Dependent Dielectric Breakdown
UNCD	Ultra-Nano-Crystalline-Diamond
UV	Ultraviolet
WS2	Tungsten Disulfide

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[1]The singular and plural of an acronym are always spelled the same.

I. INTRODUCTION

THE ability to measure, and manipulate matter at the atomic/molecular scale has led to the discovery of novel materials. A nanometer is 10^{-12} meter; a single human hair is about 8×10^5 nanometers wide.

According to the definition of The Nanoscale Science, Engineering, and Technology (NSET) Subcommittee of the National Science and Technology Council's Committee on Technology (Roco [63]), "Nanotechnology is the research, and technology development at the atomic, molecular, or macromolecular levels, in the length scale of approximately 1–100 nanometer range, to provide a fundamental understanding of phenomena, and materials at the nanoscale; and to create, and use structures, devices, and systems that have novel properties, and functions because of their small, and/or intermediate size." At this level, the physical, chemical, and biological properties of materials differ in fundamental, valuable ways from the properties of individual atoms, molecules, or bulk matter.

Over the last ten years, there has been a series of critical convergences in previously disparate technology areas. Integration of IC within complex MEMS device structures have opened vast new avenues for integrated sensor, and system technologies. Likewise, integration of functional "smart" nanomaterials into self-standing MEMS devices has dramatically widened the functional application space for miniaturized systems including microfluidic, and bio-compatible microdevices for biomedical applications.

As a consequence, the next several decades will see unprecedented levels of integration of emerging nanomaterials, nanoelectronic architectures, and nano-MEMS platforms. This will pose severe challenges for testing, reliability, and metrology techniques required to support such development. The integration of varied material, and technology approaches has, and will continue to result in the combination of heretofore field-specific testing, reliability, and metrology methodologies. For example, the adaptation of tomographic approaches pioneered in the health, and nondestructive evaluation (NDE) analysis fields to destructive focused ion beam imaging has generated significant interest for nanoscale 3D reconstruction in IC, and NEMS metrology. This type of "cross-contamination" between the traditional fields of NDE/testing/reliability, and the emerging areas of nanomaterials, nanoelectronics, and NEMS is essential to develop the metrology, and test/reliability solutions that are needed. Near-field acoustics for nanoscale mechanics & stress evaluation, near-field optics for nanoscale chemical & optical probing, and nanometer-resolved x-ray imaging are additional examples of such "cross-contamination".

Engineers are needed to help increase reliability, while maintaining effective production schedules to produce current, and future electronics at the lowest possible cost. Without effective quality control, devices dependent on nanotechnology will experience high manufacturing costs, including transistors which could result in a disruption of the continually steady Moore's law. Nanotechnology can potentially transform civilization. Realization of this potential needs a fundamental understanding of friction at the atomic scale. Furthermore, the tribological considerations of these systems are expected to be an integral aspect of the system design, and will depend on the training of both existing, and future scientists, and engineers in the nano scale (Krim [37]).

Nano-reliability measures the probability that a nano-scaled product performs its intended functionality without failure under given conditions for a specified period of time. Experience in conventional manufacturing shows that neglecting reliability in an early stage results in extremely high direct, and indirect costs on production suspension, product repair or replacement, and other loss in later stages of product lifecycles. In macro- and micro-systems, reliability has also been essential for product design, and manufacturing (see, e.g., Srikar & Senturia [70], De Wolf [18], van Spengen [77], Melle, *et al.* [50], and Choa [16]). In the promising nano-world, reliability will be even more important due to expected higher functionality, and complexity of products. As most materials exhibit totally different physical properties when operating in a nano scale, compared to larger scales, research on nano-reliability defines a new, promising area that deserves more interests.

In nano-reliability research, traditional generic reliability theories could still be applicable with proper modifications. However, new models & theories are also needed to characterize diverse behaviors that happen in the nano-world. Physical processes do not scale with size, and time. When size goes to a scale as small as micro or nano, dramatic changes in electrical conductivity, reaction kinetics, corrosion processes, etc. may be seen. Important concepts in reliability engineering, such as fatigue, friction, damping, wear-out, and repair mechanisms, have different physical meanings on atomic or molecular scales.

The reliability of nano devices is still far from perfected. Failures in micro-systems, and nano-systems can be traced back to thermal, mechanical, chemical, electrical, or combined origins thereof; which may be caused by different manufacturing stages such as wafer processing, packaging, and final assembly; and post-production stages such as transportation, and usage. Typical failures found in these systems are cracks, delamination, buckling, warpage, popcorning, stress voiding, fatigue, pattern shift, thermo-migration, and electrical stress-induced failures such as hot carrier degradation, breakdown of thin oxides, and electro-migration. The majority of these failures (65%) are thermo-mechanically related (Michel [51]).

This review coves extensively the latest progress on nano-reliability published in the following journals: Microelectronics Reliability, Microelectronic Engineering, IEEE Transactions on Device and Materials Reliability, IEEE Transactions on Nanotechnology, Proceedings of SPIE, IEEE Transactions on Electron Devices, IIE Transactions and Materials Science and Engineering, and others.

As an emerging field, research on nano-reliability is facing the following main tasks:

- Introduction of concepts, and technical terms of reliability to nano-technology in an early state.
- Identification of physical failure mechanisms of nano-structured materials, and devices during fabrication process and operation.
- Determination of quality parameters of nano-devices, failure modes, and failure analysis including reliability testing procedures, and instrumentation to localize nano-defects.
- Modeling of reliability functions, and failure rates of nano-systems.

The rest of this paper is organized as follows. Due to the promising development of nanotechnology, review work that focuses on different aspects of nanotechnology appear. Section II introduces several other review papers that are related to nano-reliability research. In reliability research, it is important to understand the types of failure-modes, and intrinsic mechanism, so Section III reviews failure-modes commonly seen in high-k films, nanostructure, MEMS, CMOS, and other nano-structured components. Manufacturing reliability, aging, and degradation models as well as failure, and lifetime models are also reviewed in this section. Section IV investigates reliability testing issues, and related evaluation & measurement techniques. Section V introduces some structure, and parameter design methodologies for nano-reliability. Finally, Section VI concludes this paper with a summary, and view of future research.

II. Related Review Work

As nanotechnology, and MEMS are enabling new discoveries in diverse fields of science, and engineering (Huff [25]), a collection of review papers have been seen recently that try to summarize the various impacts that nanotechnology is bringing. Focusing on different physical, and statistical issues, these review papers have provided a general background of reliability research in nano-engineering.

Motivated by a recent prediction made by the Semiconductor Industry Association (SIA) in the International Technology Roadmap for Semiconductors (ITRS [26]) that the silicon technology will continue its historical rate of advancement with the Moore's law for at least a couple of decades, Wong & Iwai [78] indicated that the silicon gate oxide will be scaled down to its physical limit. An alternate way is to replace oxide with a physically thicker high-k material to help solve most of the problems. However, new problems concerning reliability, and performance have to be addressed. Ribes, *et al.* [61] reviewed the status of reliability studies of high-k gate dielectrics, and illustrated some concepts with experimental results.

Stathis [71] focused on the reliability limits for the gate insulator in CMOS technology. The author reported that present research is aimed at better understanding the nature of the electrical conduction through a breakdown spot, and the effect of the oxide breakdown on device, and circuit performance. However, it is also noted that an oxide breakdown may not necessarily lead to immediate circuit failure. Therefore, more research is needed to develop a quantitative methodology for predicting the reliability of circuits. Lombardo, *et al.* [45] reviewed the subject of oxide breakdown, while focused more on the case of the gate dielectrics of interest for situations under which Si oxides or oxynitrides of thickness ranging from some tens of nanometers down to about 1 nm. Specifically, the authors investigated the kinetics of oxide degradation, and the statistics of the time to breakdown. Experimental studies were conducted to study the influential factors to oxide breakdown.

The only commercialized electronic packaging technique is still lead-bearing soldering. Challenging issues, such as lower electrical conductivity, conductivity fatigue in reliability testing, limited current-carrying capability, and poor impact strength, are not well solved by other new techniques. Li & Wong [42] gave a thorough review of the recent development in electrical conductive adhesives, and studied the electrical, mechanical, and thermal behavior improvements, as well as reliability enhancement under various conditions.

Microstructural design has attracted increasing interest in the modern development of hard coatings for wear-resistant applications. Mayrhofer, *et al.* [49] demonstrated the correlation between microstructure, mechanical properties, and tribological properties of hard ceramic coatings. The authors also noted that developments in all applications will benefit from a closer interaction of the different fields as many of the materials quality & reliability issues are similar, for example, for controller file texture, defect density, and purity.

The development of the nanotechnology has extended its impact to the degradation of solid dielectrics as well. Morshuis [53] reviewed the vast literature on partial discharge, and partial discharge induced degradation. The author emphasized that many properties of the new generation of dielectrics can be affected by the introduction of small amounts of nano-sized particles.

Electrostatic discharge (ESD) protection design for mixed-voltage I/O interfaces has been one of the key challenges of system-on-a-chip (SOC) implementation in nano-scaled CMOS processes. Ker & Lin [29] presented a broad overview on the ESD design constraints in mixed-voltage I/O interfaces, the classification & analysis of ESD protection designs for mixed-voltage I/O interfaces, and the designs of high-voltage-tolerant power-rail ESD clamp circuits.

As nanotechnology is gradually being integrated in new product design, it is important to understand the mechanical, and material properties for the sake of both scientific interest, and engineering usefulness. Kitamura, *et al.* [32] reviewed works on the strength of ideal nano-structure components. The authors also noted that a good understanding of the mechanical properties of nano-structured components is important to the design of fabrication/assembly processes, and reliability in service, which will soon be a major focus when nanotechnology is ready for massive production. Some discussion on thermally driven reliability issues in microelectronic systems can be found in the work of Lasance [39].

III. Mechanism Analysis and Modeling in Nano-Reliability

As aforementioned, failures in micro-systems, and nano-systems can be traced back to thermal, mechanical, chemical, electrical, or combined origins thereof. In this section, we review the physical, mechanical, or chemical failure modes of popular applications in the current nano-engineering research, and introduce research in the modeling of these failures.

A. Failure-Mode and Mechanism Analysis

The behavior of nanostructured materials/small-volume structures, and biological/bio-implantable materials is currently much in vogue in materials science. One aspect of this field, which has received only limited attention, is their fracture & fatigue properties. Ritchie, *et al.* [62] examined the premature fatigue failure of silicon-based micron-scale structures for MEMS, and the fracture properties of mineralized tissue, specifically human bone.

Similarly, accurate identification of mechanical properties arises whenever very thin coatings that consist of single or multiple layers are considered. Rapid developments in the areas of nano-fabrication, nano-manipulation, and nanotechnology lead to the increased importance of reliable characterization of mechanical properties of progressively thinner coatings. A recent study on this topic is Korsunsky & Constantinescui [34].

Failure analysis (FA) also plays an important role in the development, and manufacture of integrated circuits. However, instrumental limits are already causing problems in FA in the tenth-micron CMOS realm. Nanoelectronic devices will meet the problem of incapable analytical tools. Vallett [76] introduced state-of-the-art microelectronic failure analysis processes, instrumentation, and principles. The major limitations, and future prospects determined from industry roadmaps are discussed. Specifically highlighted is the need for a fault isolation methodology for failure analysis of fully integrated nanoelectronics devices.

Nanocomposites exhibit new, improved properties when compared to their micro- or macrocomposite counterparts. By lowering the particle size to nano dimensions, the special effects in polymer composites appear. Kovacevic, *et al.* [36] compared the properties of composites with micro-, and nano-sized calcium carbonate (CaCO3) particles in a poly (vinyl acetate) (PVAc) matrix. Mathematical models were used to quantify the interfacial interactions in the composites under investigation. It seems that a key characteristic of the nanocomposites is the formation of a three-dimensional interphase with a significant amount of restricted chain mobility.

Luo, *et al.* [46] examined some fundamental reliability aspects of high-k film through ramp voltage stress testing. By studying dielectric relaxation, and analysing the TRANSIENT conductivity, breakdown modes of the tested high-k film are identified; a sensitive method of breakdown detection in ramped voltage tests is proposed, and investigated.

Luo, *et al.* [47] investigated the breakdown phenomena of TiN/ZrHfO/HfSiO/p-Si, and found that defect accumulation in the interface region triggers breakdown of the stack subjected to gate injection. Luo, *et al.* [48] investigated the relaxation currents of a variety of high-k gate stacks, and obtained evidence relating relaxation properties to dielectric integrity. The authors suggested that even though relaxation current is not detectable on SiO_2, it is obvious on the high-k stacks, which signified the integrity of high-k dielectrics. The breakdown sequence of individual layers in the double-layer high-k stacks has been identified. Such findings would be valuable in understanding the breakdown of multilayer high-k stacks.

Lombardo, *et al.* [45] presented new failure mechanisms associated with breakdown in high-k gate stacks on the case of Si oxides, or oxynitrides of thickness ranging from some tens of nanometers down to about 1 nm. In addition to dielectric-breakdown-induced epitaxy commonly found in breakdowns in poly-Si/SiON, and poly-Si/Si_3N_4 MOSFETs, grain-boundary, and field-assisted breakdowns near the poly-Si edge are found. The authors also developed a model based on breakdown induced thermo-chemical reactions to describe the physical microstructural damages triggered by breakdown in the high-k gate stack, and the associated post-breakdown electrical performance.

Bae, *et al.* [2] provided basic physical modeling for MOSFET devices based on the nano-level degradation that takes place at defect sites in the MOSFET gate oxide. The authors investigated the distribution of hot-electron activation energies, and derived a logistic mixture distribution using physical principles on the nanoscale.

Basaran, *et al.* [4] qualified the damage mechanism in solder joints in electronic packaging under thermal fatigue loading through experiments. The authors also showed that damage MECHANISMS under thermal cycling are very different than those under mechanical cycling. Elastic modulus degradation under thermal cycling, which is considered as a physically detectable quantity of material degradation, was measured using a nano-indenter.

Tomczak, *et al.* [74] presented the use of single molecules to study local, and nanoscale polymer dynamics. Fluorescence lifetime fluctuations were used to extract the number of polymer segments taking part in the rearranging volume around the probe molecule below the glass transition temperature. It was found that the number of polymer segments decreased with increasing temperature.

B. Manufacturing Reliability

The development of nanotechnology will lead to the introduction of new products to the public. In the modern large-scale manufacturing era, reliability issues have to be studied; and results incorporated into the design, and manufacturing phases of new products.

Kitamura, *et al.* [32] pointed out that some nano structured components, including nano films, nano tubes, and nano clusters, are very reliable once manufactured. Such components show high strength characteristics. However, their manufacturing procedures are complicated. Moreover, utilizing the structure at the nano level is a key technology in the development of electronic devices, and elements of nano electro-mechanical systems. Therefore, it is important to understand the mechanical properties for engineering usefulness, such as design of fabrication processes, to produce these components effectively. Lee, *et al.* [40] discussed the critical issues of MEMS in four categories: functional interfaces, reliability, modeling, and integration. They conducted burn-ins, and accelerated tests to ensure the production of a reliable MEMS device. In the nanofabrication of solid materials, Klein-Wiele, *et al.* [33] found that there is a quality & reliability advantage of the combination of femtosecond pulse durations with ultraviolet wavelengths in the nanofabrication of solid materials.

Kouvelis & Mukhopadhyay [35] analyzed failures, such as access time failure, read/write stability failure, and hold stability failure in the stand-by mode of SRAM cells due to process parameter variations; and they modeled the failure probabilities. A method to predict the yield of a SRAM memory chip designed with a cell is proposed based on the cell failure probability. The developed method can be used in the early stage of a design cycle to optimize the design for yield enhancement.

As one of the critical procedures in semiconductor manufacturing, nanoimprint lithography is seen as an alternative to conventional nanometer scale patterning technologies like electron beam lithography. Finder, *et al.* [19] introduced that nanoimprint lithography is a low cost method for the fabrication of nano-scaled patterns. The parallel process involves a stamp pressing into a softened polymer layer. This method has demonstrated high reliability, high throughput, and low cost. It has been used to print on 6 inches wafers, and has demonstrated the ability to master nanostructures down to 10 nm.

On-chip integrated MIM capacitors are finding increasing attention for various applications in advanced high performance mixed signal, and RF products. Typical requirements include low area consumption, large specific capacitance, low capacitance tolerances, high quality factors, and low parasitic substrate coupling. Schrenk, *et al.* [66] presented an approach for integrating MIM caps into a copper multilevel metallization using Cu lines as a bottom electrode for the capacitor.

Sikora, *et al.* [68] examined the various technologies for implementing embedded flash cells. By focusing on automotive application, the authors discussed the technological basics with regard to practical consequences, and concentrated on the aspects of reliability of embedded flash cells. The required process steps are presented as well as the test approaches to ensure a high-quality production level.

Ganesan, *et al.* [20] utilized multi-scale wavelet SPC to analyze the quality of chemical mechanical planarization of silicon wafers in production. The wavelet method allows for real-time defect detection during manufacturing on the nano scale. By integrating with an advanced SPC method, individual defects could be differentiated simultaneously as they occur in the chemical mechanical planarization processing.

C. Aging and Degradation Models

The aging, and degradation effects are the major reasons that lead to product failures. In this section, research on photodegradation, oxide breakdown, and other aging & degradation models are reviewed.

Sivalingam & Madras [69] analyzed the mechanism of photodegradation. Product degradation was detected using UV-Visible spectroscopy, FT-IR, and GC/MS. The mechanism of breakage during photocatalytic degradation can be attributed to concerted rearrangement (Photo-Fries), and non-concerted cage recombination (oxidation). The degradation was measured by the molecular weight distribution using gel permeation chromatography (GPC), and modeled with continuous kinetics distribution.

Liu, *et al.* [44] developed a model accounting for oxide breakdown. Data measured on the nMOS transistor biased in the linear region before, and after breakdown are used to extract the breakdown spot resistance, and total gate capacitance. This methodology provides critical information about the impact brought by gate oxide breakdown.

Lin, *et al.* [43] proposed a new sub-circuit degradation model. The reliability of class-E, and class-A power amplifiers is investigated. Experimental results of degradation characteristics on the fabricated circuits agree well with the simulation predictions. From this newly developed model, the authors found that the class-E amplifier degrades faster than a class-A amplifier. A shorter lifetime is expected for a class-E amplifier.

Umemura, *et al.* [75] clarified the degradation behavior of the electric double layer capacitors. The authors identified that the capacitance decrease might be caused by the degradation of the electrolysis, propylene carbonate, and also the degradation by-products which piled on the nano-scaled micro-cavity surface of the activated-carbon particles of the electrodes. The degradation mechanism was found to be governed by the Arrhenius chemical kinetics theory, and consisted of two stages with different activation energies.

Cester, *et al.* [10], and Miranda & Jimenez [52] investigated the breakdown dynamics of ultrathin SiO_2 films in metal-oxide-semiconductor structures. It was shown that the progressive increase of the leakage current that flows through the oxide when subjected to constant electrical stress can be modeled by the stochastic logistic differential equation. This approach relies on a time-scale separation in which a deterministic term provides the S-shaped growth trajectory, while a second term of the equation deals with the noisy behavior. Because of the inherent mean reverting property of the simulation process, the proposed model is also able to cover cases in which sudden upward, and downward changes of the system's conductance are registered.

By combining the oxide time to breakdown model with a defect size distribution, Kim, *et al.* [30] presented a model to tie oxide yield to time-dependent reliability. Cester, *et al.* [10] presented an original model to explain the accelerated wear-out behavior of irradiated ultra-thin oxides. The model uses a statistical approach to model the breakdown occurrences based on a non-homogeneous Poisson process.

Suehle, *et al.* [73] studied two post soft-breakdown modes: one in which the conducting filament is stable until hard breakdown, and one in which the filament continually degrades with time. Acceleration factors are different for each mode, indicating different physical mechanisms. The results suggest that the "hardness" of the first breakdown influences the residual time distribution of the following hard breakdown. Tunneling current appears to be the driving force for both modes.

In practice, degradation processes do not all occur in a continuous pattern. Hsieh & Jeng [24] established a procedure for accessing the reliability using a discrete model. A non-homogeneous Weibull compound Poisson model with accelerated stress variables is considered by the authors. A dataset measuring the leakage current of nanometer-scale gate oxides is analyzed by using this procedure.

Chen & Ma [14] examined in-vitro hydrolytic degradation behavior for nano-fibrous (NF) poly (L-lactic acid) (PLLA) foams prepared by phase separation. In their research, nano-fibrous foams were incubated in phosphate-buffered saline at 371° C for 15 months. Upon removal, changes in mass, molar mass, morphology, BET specific surface area, mechanical properties, and thermal properties were compared with those of similarly incubated solid-walled (SW) PLLA foams. The initial surface area in NF foams was over 80 times higher than in SW foams. During incubation, NF surface area decreased steadily, only possessing 17% of the original specific surface area after 15 months, and SW surface area stayed constant throughout.

Polymer additives often show many side reactions during the aging of polymers, which changes the useful lifetime of materials. Side reactions have been found in nano-grade titanium dioxide additives. The interaction between titanium dioxide pigments, and stabilizers therefore is proposed as a field of great importance. Zeynalov & Allen [79] investigated the influence of nano, and micron particle grade anatase; and rutile titanium dioxide pigments on the efficiency of a hindered amine stabilizer. Bressers, *et al.* [9] presented some results of models to link the chemical details of polymers, and microelectronic reliability.

Kufluoglu & Alam [38] investigated Negative Bias Temperature Instability (NBTI)- induced degradation for ultra-scaled, and future-generation MOSFET. Numerical simulations based on Reaction-Diffusion framework were implemented. Geometric dependence of degradation arising from the transistor structure & scaling is incorporated into the model. The simulations are applied to narrow-width planar triple-gate, and surround-gate MOSFET geometries to estimate the NBTI reliability under several scaling scenarios. Unless the operating voltages are optimized for specific geometry of transistor cross section, the results imply worsened NBTI reliability for the future-generation devices based on the geometric interpretation of the NBTI degradation. A time-based model is developed to predict the degradation.

D. Failure and Lifetime Models

Failures, and lifetime models are important to lifetime forecasting, and design for reliability. Research on such models for CMOS, digital micromirror devices, nanotubes, and other important nano-devices are recently seen in the literature.

Schwalke, *et al.* [67] investigated the breakdown of extra thick gate oxides (50–150 nm) used in power MOS devise. Weibull probability plots are used to describe the failure distribution of the thick gate oxides.

Groeseneken, *et al.* [21] reviewed an acceleration model. Recent trends of reliability assessment in CMOS were also discussed. Lee, *et al.* [41] investigated the possibility of integrating chemical vapor deposition (CVD) HfO_2 into the multiple gate dielectric SOC process in the range of 6–7 nm. They predicted the ten-year time-dependent dielectric breakdown (TDDB) reliability of HfO/SiO_2 gate stack.

Namazu & Isono [54] studied the effects of specimen size, frequency, and temperature on fatigue lives of nanoscale single crystal silicon (SC-Si), and silicon dioxide (SiO_2) wires for reliable design of micro/nano electromechanical systems. Evaluation of fatigue lives for nanoscale fixed SC-Si, and Si02 wires was performed by stress-controlled cyclic bending tests under an atomic force microscope (AFM) at temperatures ranging from 295 K to 573 K. In MEMS-00, and MEMS-01, the quasi-static bending tests under the AFM for nanoscale SC-Si wires were reported.

Barber, *et al.* [3] summarized, and discussed the limited statistically significant, currently available, experimental data for the tensile strength of individual nanotubes of any sort. Only three such data sets currently exist: two for multi-wall carbon nanotubes, and one for multi-wall WS2 nanotubes. It is shown by the authors that Weibull-Poisson statistics accurately fit all strength data sets, and thus seem to apply at the nano scale as well as at the micro/macro-scales.

Jean, *et al.* [27] used positron annihilation spectroscopy (PAS), coupled with a variable mono-energetic positron beam, to investigate surface, and interfacial properties in thin polymeric films. The authors measured free-volume properties from ortho-Positronium lifetime, and the S parameter of Doppler broadening of energy spectra from annihilation radiation as a function of the depth and temperature in thin polymeric films. They also presented glass transition temperature profile on nanoscale layered structures in polystyrene (PS) thin films.

Reliability of magnetic tunnel junctions emerges as a critical problem for the successful application of the new writing schemes to the next generation high-density MRAM devices. Kim, *et al.* [31] presented reliability characteristics, and the thermal stability of magnetic tunnel junctions. The Weibull distribution is used for the data fitting.

Chasiotis & McCarty [11] described strength data for uniformly stressed MEMS specimens. The Weibull model has been used extensively. The authors investigated the relevance of the Weibull model to more general situations of MEMS-scale specimen failure. The applicability of the Weibull model for describing the failure of (a) specimens with a single flaw distribution, and variable geometry; and (b) multiple flaw populations, and a specific geometry is studied.

IV. Reliability Testing and Evaluation

Reliability testing of nano-devices is important in nano-reliability research. This section reviews techniques used for films, wafers, nanocomposite materials, and other nano-products.

A. Reliability Testing

Thin films, and coatings can fail by fatigue at lower loads than predicted by static tests. Beake & Smith [5] introduced a nano-impact technique, which is a low load impact test capable of revealing remarkable differences in performance useful in optimizing the design of coating systems for improved durability. In particular, the proposed technique can be used to find the optimum coating process parameters for enhanced toughness, and damage tolerance; and also differentiate between cohesive (chipping), and adhesive failure (delamination).

Chen, *et al.* [13] investigated the reliability of anodically-bonded packages between silicon, and borosilicate glass wafers. Effects of certain accelerated environmental tests such as thermal cycling, thermal shock, and boiling test on bonding quality are evaluated. Bonding strength is measured using an in-house tensile tester. The fact that fracture mainly occurs inside the glass wafer rather than along the interface indicates the robustness of the bond.

Pervin, *et al.* [58] developed a novel technique to fabricate nano-composite materials containing SC-15 epoxy resin, and carbon nano fiber (CNF). A high-intensity ultrasonic liquid processor was used to obtain a homogeneous molecular mixture of epoxy resin, and carbon nano fiber. Based on the experimental results, a nonlinear damage model was established to describe the stress-strain relationship of the epoxy, and its nano-composite.

Cheung [15] noted that solid-insulator breakdown always leads to an irreversible permanent conduction path. This is a key assumption in all gate-oxide breakdown reliability assessment, and lifetime projection. This assumption is not valid when the gate-oxide thickness is less than 2 nm, and the operation voltage is 1 V or less. Chatterjee, *et al.* [12] investigated the dielectric breakdown property of ultrathin 2.5, and 5.0 nm hafnium oxide (HfO_2) gate dielectric layers with metal nitride (TaN) gate electrodes for MOS structure. Reliability studies were performed with constant voltage stress to verify the effects of changing processing conditions (film thicknesses, and post metal annealing temperatures) on time to breakdown. The leakage current characteristics are improved with post metal annealing (PMA) temperatures for both 2.5, and 5.0 nm thicknesses HfO_2.

B. Reliability Evaluation and Measurement Techniques

Measurement, and evaluation of reliability of nano-devices is an important subject. New technology is developed to support the achievement of this task.

As noted by Keller, *et al.* [28], with ongoing miniaturization from MEMS towards NEMS, there is a need for new reliability concepts making use of meso-type (micro to nano) or fully nano-mechanical approaches. Experimental verification will be the major method for understanding theoretical models, and simulation tools. Therefore, there is a need for developing measurement techniques which have capabilities of evaluating strain fields with very local (nanoscale) resolution.

Peng & Cho [57] proposed the concept of a new type of nanoscale sensor devices that can detect the presence of CO, and water molecules. To overcome the reliability problem, these devices were developed by substitution-doping of impurity atoms (such as boron, or nitrogen atoms) into intrinsic single-wall carbon nanotubes, or by using composite nanotubes. Keller, *et al.* [28] developed the nanoDAC method (nano Deformation Analysis by Correlation), which enables the extraction of nanoscale displacement fields from scanning probe microscopy (SPM) images.

Su, *et al.* [72] used the Pearson correlation coefficient to calculate the digital speckle correlation for nano-metrology, which can be applied to MEMS, and IC packaging. Bhaduri & Shukla [7] used a Markov Random Field as a model of computation for nanoscale logic gates. They take the approach further by automating this computational scheme using a Belief Propagation algorithm (Pearl [56]).

Bhaduri & Shukla [8], and Bhaduri & Shukla [6] extended previous work on evaluating reliability-redundancy trade-offs for NAND multiplexing to trade-offs among granularity, redundancy, and reliability for several redundancy mechanisms; and presented their automation mechanism using the probabilistic model checking tool PRISM. Nano computing in the form of quantum, molecular, and other computing models is proliferating as nano fabrication advances. With the advance to nano scale fabrication, unprecedented levels of defects arise. Their MATLAB-based tool NANOLAB helps to uncover the anomalies during fabrication, thereby providing better insight into defect tolerant design decisions.

Norman, *et al.* [55] evaluated the reliability of defect-tolerant architectures for nanotechnology with probabilistic model checking.

Holmberg [23] dealt with the role of tribology in the large, complex scope of reliability engineering. They discussed different tribology-related methods for improving product reliability, such as reliability design, component lifetime, condition monitoring, and diagnostics. Cumulative wear, and change of friction were recorded through time.

Zhihong, *et al.* [81] presented the methodology of the reliability modeling, and simulation for the state-of-the-art nanotechnology; and discussed the extraction for HCI (Hot Carrier Injection), and NBTI (Negative Bias Temperature Instability) for product lifetime models. The integration of these models into the transistor level, and gate level simulation flow can be used by the designers to satisfy product reliability requirements.

V. Structure and Parameter Design for Reliability

Due to the high reliability-related cost, structure & parameter design techniques can be employed to minimize possible loss due to poor quality nano-devices. The following work provides useful examples of design-for-reliability in nano-engineering.

Zhao, *et al.* [80] presented a "Noise Impact Analysis" methodology to evaluate the transient error effects in static CMOS digital circuits. A "Noise Capture Raito" has been defined by the authors to measure the transient noise effects in the circuit. The proposed methodology facilitates the economic design of robust nanometer circuit.

Prabhakumar, *et al.* [59] described the assembly, and reliability of flip chips with a nano-filled wafer. They use Box-plots to compare the underfill interface distributions, and conducted a reliability test for failure mechanisms.

Nanotechnology in static random access memory (SRAM) cells is also advancing. SRAM is much more reliable than dynamic RAM, and allows for access time to be much quicker. Agarwal, *et al.* [1] conducted experimental analysis of the impact of process variation on the different failure mechanisms in SRAM cells on a sixty-four K cache. The authors proposed a process tolerant cache architecture, which can achieve ninety-four percent yield compared to its original thirty-three percent yield (standard cache) in the forty-five nanometer predictive technology. This technique surpasses all the contemporary fault tolerant schemes such as row-column redundancy, and ECC in handling failures due to process variation.

Pugno, *et al.* [60] used an experimental-theoretical method to investigate the strength of structures having complex geometries, which is commonly used in MEMS. It involves the stretching to failure of freestanding thin film membranes, in a fixed configuration, containing micro fabricated sharp cracks, blunt notches, and re-entrant corners. The defects, made by nano-indentation, and focused ion beam milling, are characterized by scanning electron microscopy (SEM). MEMS structures made of ultra-nano-crystalline-diamond (UNCD) were investigated using this methodology. A theory to predict the strength of micro structures with defects was proposed, and compared with experimental results. It was shown that the concepts of fracture mechanics can be applied with confidence in the design of MEMS.

Schmid & Leblebici [65] discussed various circuit-, and system-level design challenges for nanometer-scale devices, and single-electron transistors, with an emphasis on the functional robustness, and fault tolerance point of view. A set of general guidelines is identified for the design of very high-density digital systems using inherently unreliable, error-prone devices.

Cotofana, *et al.* [17] introduced a design methodology that allows the system/circuit designer to build reliable systems out of unreliable nano-scaled components. The central point of the proposed approach is a generic (parametrical) architectural template, which is named configurable nanostructures for reliable Nano electronics (CONAN). CONAN embeds support for reliability at various levels of abstractions. Han & Jonker [22] developed the probability of the system survival of a defect-, and fault-tolerant architecture for nano-computers.

Motivated by the need for economical fault-tolerant designs for nano-architectures, Roy & Beiu [64] explored a novel multiplexing-based redundant design scheme with redundancy factors, R, at small $(\mathrm{R} \leq 100)$ and very small $(\mathrm{R} \leq 10)$ levels. In particular, the authors adapted a strategy known as von Neumann multiplexing to circuits of majority gates with three inputs, and analyzed the performance of a multiplexing scheme for very small redundancies using combinatorial arguments.

VI. Conclusions

The behavior of nano-scaled products is much more sensitive to changes in material compositions, manufacturing controllable variables, and noise parameters. This paper has reviewed various aspects of reliability research in the emerging nanotechnology. Around 80 papers from nearly 40 leading journal in nano-related areas have been covered, including 10 review papers summarized in Section IV.

We have broken down our presentation into the following four main topics:

- Introduction of concepts, and technical terms of reliability to nano-technology.
- Identification of physical failure mechanisms of nano-structured materials, and devices.
- Determination of quality parameters of nano-devices, failure modes, and failure analysis including reliability testing procedures, and instrumentation to localize nano-defects.
- Modeling of reliability functions, and failure rates of nano-systems.

Much work is needed in the nano-reliability field to ensure the product reliability, and safety in various use conditions.

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